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Search Results - Record(s) 1 through 11 of 11 returned.

☐ 1. Document ID: US 20040103111 A1

Using default format because multiple data bases are involved.

L5: Entry 1 of 11 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040103111
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040103111 A1

TITLE: Method and computer program product for determining an area of importance in an image using eye monitoring information

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Miller, Michael E.	Rochester	NY	US
Cerosaletti, Cathleen D.	Rochester	NY	US
Fedorovskaya, Elena A.	Pittsford	NY	US
Covannon, Edward A.	Ontario	NY	US

US-CL-CURRENT: 707/102

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 20030204488 A1

L5: Entry 2 of 11 File: PGPB Oct 30, 2003

PGPUB-DOCUMENT-NUMBER: 20030204488
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030204488 A1

TITLE: Management system, management method and apparatus, and management apparatus control method

PUBLICATION-DATE: October 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Sentoku, Koichi	Tochigi		JP
Ina, Hideki	Kanagawa		JP
Suzuki, Takehiko	Saitama		JP

Matsumoto, Takahiro	Tochigi	JP
Oishi, Satoru	Tochigi	JP

US-CL-CURRENT: 707/1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 3. Document ID: US 20030069885 A1

L5: Entry 3 of 11 File: PGPB Apr 10, 2003

PGPUB-DOCUMENT-NUMBER: 20030069885
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030069885 A1

TITLE: Integrated service platform

PUBLICATION-DATE: April 10, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Chang, Da-Yi	Kaohsiung		TW
Lin, Chun-Hung	Hsinchu		TW
Li, Kun-Pei	Miaoli		TW
Ting, Hsiu-Lan	Hsinchu		TW
Tu, Kung-Cheng	Kaohsiung		TW
Sun, Mao-Shing	Taipei		TW

US-CL-CURRENT: 707/10

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 4. Document ID: US 20030061212 A1

L5: Entry 4 of 11 File: PGPB Mar 27, 2003

PGPUB-DOCUMENT-NUMBER: 20030061212
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030061212 A1

TITLE: Method and apparatus for analyzing manufacturing data

PUBLICATION-DATE: March 27, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Smith, Shawn B.	Palo Alto	CA	US
Grigsby, Brian P.	Austin	TX	US
Pham, Hung J.	Leander	TX	US

Davis, Tony L.	Austin	TX	US
Yedatore, Manjunath S.	Austin	TX	US
Clements, William R. III	Austin	TX	US

US-CL-CURRENT: 707/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 20010047222 A1

L5: Entry 5 of 11 File: PGPB Nov 29, 2001

PGPUB-DOCUMENT-NUMBER: 20010047222
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010047222 A1

TITLE: Reticle management system

PUBLICATION-DATE: November 29, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Wiesler, Oren	Wayland	MA	US
Mariano, Thomas	Londonderry	NH	US

US-CL-CURRENT: 700/214; 700/121, 707/100, 716/21

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 6965895 B2

L5: Entry 6 of 11 File: USPT Nov 15, 2005

US-PAT-NO: 6965895
DOCUMENT-IDENTIFIER: US 6965895 B2

TITLE: Method and apparatus for analyzing manufacturing data

DATE-ISSUED: November 15, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Smith; Shawn B.	Palo Alto	CA		
Grigsby; Brian P.	Austin	TX		
Pham; Hung J.	Leander	TX		
Davis; Tony L.	Austin	TX		
Yedatore; Manjunath S.	Austin	TX		
Clements, III; William R.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Applied Materials, Inc.	Santa Clara	CA			02

APPL-NO: 10/194920 [PALM]
DATE FILED: July 12, 2002

PARENT-CASE:
This application claims the benefit of: (1) U.S. Provisional Application No. 60/305,256, filed on Jul. 16, 2001; (2) U.S. Provisional Application No. 60/308,125, filed on Jul. 30, 2001; (3) U.S. Provisional Application No. 60/308,121 filed on Jul. 30, 2001; (4) U.S. Provisional Application No. 60/308,124 filed on Jul. 30, 2001; (5) U.S. Provisional Application No. 60/308,123 filed on Jul. 30, 2001; (6) U.S. Provisional Application No. 60/308,122 filed on Jul. 30, 2001; (7) U.S. Provisional Application No. 60/309,787 filed on Aug. 6, 2001; and (8) U.S. Provisional Application No. 60/310,632 filed on Aug. 6, 2001, all of which are incorporated herein by reference.

INT-CL-ISSUED: [07] G06 F 17/30

US-CL-ISSUED: 707/10; 707/5, 707/6, 707/101, 707/104.1, 706/25
US-CL-CURRENT: 707/10; 706/25, 707/101, 707/104.1, 707/5, 707/6

FIELD-OF-CLASSIFICATION-SEARCH: 707/5, 707/6, 707/10, 707/101, 707/104.1, 707/1, 707/3, 707/103Y, 706/11, 706/12, 706/16, 706/25, 706/26, 706/44, 715/854
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5097141	March 1992	Leivian et al.	706/12
5222210	June 1993	Leivian et al.	715/854
5692107	November 1997	Simoudis et al.	395/50
5819245	October 1998	Peterson et al.	706/16
5897627	April 1999	Leivian et al.	706/12
5926809	July 1999	Szalwinski	707/3
6571227	May 2003	Agrafiotis et al.	706/15
6839713	January 2005	Shi et al.	707/101
6878517	April 2005	Benson	435/6

OTHER PUBLICATIONS

"Mining semiconductor manufacturing data for productivity improvement . . . " by R. M. Dabbas et al. in Computers in Industry, vol. 45. pp. 29-44, May 2001.
"Solving Tough Semiconductor Manufacturing Problems Using Data Mining" by R. Gardner et al. IEEE/SEMI Advanced Semiconductor Manuf. Conf. Sep. 12, 2000, pp. 46-55.
"Yield Analysis and Data Management Using Yield Manager" by F. Lee et al., IEEE/SEMI Advanced Semiconductor Manuf. Conf. Sep. 22-25, 1998, pp. 19-30.
"Architecture of Data Mining Server: DATAFRONT/Serveer" by H. Ashida et al. Systems, Man and Cybernetics, 1999, IEEE SMC '99 Conference Proc. Oct. 12, 1999 pp. 882-887.

ART-UNIT: 2162

PRIMARY-EXAMINER: Alam; Shahid

ATTY-AGENT-FIRM: Stern; Robert J.

ABSTRACT:

A method for data mining information obtained in an integrated circuit fabrication factory ("fab") that includes steps of: (a) gathering data from the fab from one or more of systems, tools, and databases that produce data in the fab or collect data from the fab; (b) formatting the data and storing the formatted data in a source database; (c) extracting portions of the data for use in data mining in accordance with a user specified configuration file; (d) data mining the extracted portions of data in response to a user specified analysis configuration file; (e) storing results of data mining in a results database; and (f) providing access to the results.

24 Claims, 26 Drawing figures

☐ 7. Document ID: US 6789079 B2

L5: Entry 7 of 11 File: USPT Sep 7, 2004

US-PAT-NO: 6789079
DOCUMENT-IDENTIFIER: US 6789079 B2

TITLE: Integrated service platform

DATE-ISSUED: September 7, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chang; Da-Yi	Kaohsiung			TW
Lin; Chun-Hung	Hsinchu			TW
Li; Kun-Pei	Miaoli			TW
Ting; Hsiu-Lan	Hsinchu			TW
Tu; Kung-Cheng	Kaohsiung			TW
Sun; Mao-Shing	Taipei			TW

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Macronix International Co., Ltd.				TW	03

APPL-NO: 09/971842 [PALM]
DATE FILED: October 5, 2001

INT-CL-ISSUED: [07] G06 F 17/30

US-CL-ISSUED: 707/10; 707/3, 707/100, 709/225
US-CL-CURRENT: 707/10; 707/100, 707/3, 709/225

FIELD-OF-CLASSIFICATION-SEARCH: 707/1-10, 707/100-104.1, 707/200-206, 709/223-227, 713/202, 700/96, 700/91
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5918232	June 1999	Pouschine et al.	707/103R
6012067	January 2000	Sarkar	707/103R
6125363	September 2000	Buzzeo et al.	707/100
6295535	September 2001	Radcliffe et al.	707/10

OTHER PUBLICATIONS

Martin Hard Wick et al., Sharing Manufacturing Information in Virtual Enterprises, Feb. 1996, Communications of the ACM, 46-54.

ART-UNIT: 2172

PRIMARY-EXAMINER: Alam; Shahid

ASSISTANT-EXAMINER: Fleurantin; Jean Bolte

ATTY-AGENT-FIRM: Dickinson Wright PLLC

ABSTRACT:

The present invention discloses an integrated service platform (ISP). Under the real-time mode, the ISP of the present invention comprises the devices of: an engineering data analysis database (EDB); an area controller database (AC Database); a web server; and client computers. Under the mode of accessing data in a certain period of time, the present invention comprises the devices of: an EDB; an AC Database; a loader; a web server; and client computers. The application of the ISP of the present invention allows users on the client sites to access the data they want with browsers. Thus, no disturbance of the maintenance on the client sites would occur, because the browsers are used for accessing the data.

11 Claims, 3 Drawing figures

8. Document ID: US 6735493 B1

L5: Entry 8 of 11 File: USPT May 11, 2004

US-PAT-NO: 6735493
DOCUMENT-IDENTIFIER: US 6735493 B1
**** See image for Certificate of Correction ****

TITLE: Recipe management system

DATE-ISSUED: May 11, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chou; Alton	Jubei			TW
Wei; Chen-Hsien	Namton			TW

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Taiwan Semiconductor Manufacturing Co., Ltd.	Hsin-Chu			TW	03

APPL-NO: 10/274575 [PALM]
DATE FILED: October 21, 2002

INT-CL-ISSUED: [07] G06 F 19/00

US-CL-ISSUED: 700/121; 700/96, 700/110, 707/203, 717/170
US-CL-CURRENT: 700/121; 700/110, 700/96, 707/203, 717/170

FIELD-OF-CLASSIFICATION-SEARCH: 700/26, 700/27, 700/96, 700/109, 700/110, 700/117, 700/121, 707/203, 717/170-173, 717/168
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5761064	June 1998	La et al.	700/110
5896294	April 1999	Chow et al.	700/121
6035293	March 2000	Lantz et al.	707/1
6165805	December 2000	Steffan et al.	438/14
6185474	February 2001	Nakamura et al.	700/121
6415193	July 2002	Betawar et al.	700/97
6465263	October 2002	Coss et al.	438/14
2002/0183950	December 2002	Fu et al.	702/84
2003/0204281	October 2003	Su et al.	700/108

OTHER PUBLICATIONS

W. Jarret Campbell, PH. D., "Run-to-Run Control of Photolithography Processes," Special Focus Lithography, Yield Management Solutions, Summer 2000, pp. 65-68.

ART-UNIT: 2125

PRIMARY-EXAMINER: Picard; Leo

ASSISTANT-EXAMINER: Rodriguez; Paul

ATTY-AGENT-FIRM: Duane Morris LLP

ABSTRACT:

A recipe management system is provided including a processor configured to receive a first job file for a processing tool through a network, said first job file including a master job file for said processing tool. The processor also receives a second job file through the network from a host processor associated with the processing tool. The processor compares the first and second job files, wherein the processor determines whether the first and second job files differ. A semiconductor manufacturing method is also provided. A first job file including a master job file for a processing tool is received through a network. A second job file is also received through the network from a host processor associate with the processing tool The job files are then compared to determine whether the first and second job files differ.

27 Claims, 3 Drawing figures

☐ 9. Document ID: US 6564171 B1

L5: Entry 9 of 11 File: USPT May 13, 2003

US-PAT-NO: 6564171
DOCUMENT-IDENTIFIER: US 6564171 B1

TITLE: Method and apparatus for parsing event logs to determine tool operability

DATE-ISSUED: May 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Peterson; Anastasia Oshelski	Austin	TX		
Edwards; Richard	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices Inc.	Austin	TX			02

APPL-NO: 09/661694 [PALM]
DATE FILED: September 14, 2000

INT-CL-ISSUED: [07] G06 F 17/60, G06 F 17/30

US-CL-ISSUED: 702/182; 235/379, 370/463, 375/13, 705/1, 702/182, 707/103R, 709/228
US-CL-CURRENT: 702/182; 235/379, 370/463, 705/1, 707/103R, 709/228

FIELD-OF-CLASSIFICATION-SEARCH: 702/84, 702/177, 702/182, 702/185, 702/186, 702/119, 700/65, 700/110, 700/247, 395/75, 395/76, 395/680, 395/682, 370/463, 375/13, 705/1, 707/13R
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5412758	May 1995	Srikanth et al.	706/59
5452218	September 1995	Tucker et al.	700/110
5455894	October 1995	Conboy et al.	700/247
5465221	November 1995	Merat et al.	702/83
5488648	January 1996	Womble	375/13
5701488	December 1997	Mulchandani et al.	717/128
5757673	May 1998	Osheiski et al.	702/182
5790431	August 1998	Ahrens et al.	709/104
5981478	November 1999	Gill et al.	235/379
5999908	December 1999	Abelow	705/1
6144967	November 2000	Nock	707/103R
6317793	November 2001	Toyosawa	709/228
6370154	April 2002	Wickham	370/463

ART-UNIT: 2863

PRIMARY-EXAMINER: Barlow; John

ASSISTANT-EXAMINER: Le; John

ATTY-AGENT-FIRM: Williams, Morgan & Amerson PC

ABSTRACT:

A method for determining operability of a tool includes generating an event log including a plurality of events associated with the operation of the tool; parsing the event log to identify a crucial event; and initiating an automatic corrective action in response to identifying a crucial event. A manufacturing system includes a tool and a tool monitor. The tool is adapted to generate an event log including a plurality of events associated with the operation of the tool. The tool monitor is adapted to parse the event log to identify a crucial event and initiate an automatic corrective action in response to identifying a crucial event.

33 Claims, 2 Drawing figures

10. Document ID: US 6496747 B1

L5: Entry 10 of 11 File: USPT Dec 17, 2002

US-PAT-NO: 6496747
DOCUMENT-IDENTIFIER: US 6496747 B1
**** See image for Certificate of Correction ****

TITLE: Semiconductor device manufacturing apparatus and information processing system therefor

DATE-ISSUED: December 17, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Suzuki; Daisuke	Utsunomiya			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 09/413329 [PALM]
DATE FILED: October 12, 1999

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-304715	October 13, 1998

INT-CL-ISSUED: [07] G06 F 19/00, G06 F 17/30, H01 L 21/00

US-CL-ISSUED: 700/102; 700/99, 700/121, 438/5, 707/203
US-CL-CURRENT: 700/102; 438/5, 700/121, 700/99, 707/203

FIELD-OF-CLASSIFICATION-SEARCH: 700/3, 700/11, 700/12, 700/27, 700/99-102, 700/121, 438/5, 707/203
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5838565	November 1998	Hsieh et al.	700/100
6000830	December 1999	Asano et al.	700/100
6035293	March 2000	Lantz et al.	707/1
6115640	September 2000	Tarumi	700/100
6134482	October 2000	Iwasaki	414/14
6148246	November 2000	Kawazome	700/106
6175777	January 2001	Kim	700/121
6230068	May 2001	Wu et al.	379/14
6349287	February 2002	Hayashi	700/103

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	CLASS
08-045929	February 1996	JP	

ART-UNIT: 2125

PRIMARY-EXAMINER: Picard; Leo

ASSISTANT-EXAMINER: Frank; Elliot

ATTY-AGENT-FIRM: Fitzpatrick, Cella, Harper & Scinto

ABSTRACT:

A semiconductor manufacturing system for performing a predetermined process in accordance with a job file having a process content set therein. The manufacturing system includes a storage device for memorizing a job file, an accepting device for accepting a job file, a correction device for correcting, on the basis of a process content of a job file already memorized, a process content set in a job file as newly accepted, and a predicting device for predicting a time for completion of the process, on the basis of the job file as already memorized and the job file having its process content corrected by the correction device.

13 Claims, 8 Drawing figures

☐ 11. Document ID: US 6334215 B1

L5: Entry 11 of 11 File: USPT Dec 25, 2001

US-PAT-NO: 6334215
DOCUMENT-IDENTIFIER: US 6334215 B1

TITLE: Methodology for migration of legacy applications to new product architectures

DATE-ISSUED: December 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Barker; Brian C.	Poughkeepsie	NY		
Hartswick; Perry G.	Millbrook	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 09/305431 [PALM]
DATE FILED: May 5, 1999

INT-CL-ISSUED: [07] G06 F 9/445

US-CL-ISSUED: 717/11; 717/4, 717/5, 717/7, 707/4
US-CL-CURRENT: 717/167; 707/4, 717/176

FIELD-OF-CLASSIFICATION-SEARCH: 717/11, 717/4, 717/5, 717/7, 707/4, 707/100, 709/231, 710/126
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5359730	October 1994	Marron	717/11
5806067	September 1998	Connor	707/100
5815149	September 1998	Mutschler, III et al.	345/335
5828897	October 1998	Kirsch et al.	712/43
5899990	May 1999	Maritzen et al.	707/4
6223180	April 2001	Moore et al.	707/100
6247172	June 2001	Dunn et al.	717/5
6253244	June 2001	Moore et al.	709/231
6266729	July 2001	Leung et al.	710/126

OTHER PUBLICATIONS

Title: Managing Semantic Heterogeneity in Databases: A Theoritical Perspective, Author: Hull et al, ACM, 1997.*
Title: Reuse of Off-the_shelf Components in C2 -Style Architecutres, Authour: Medvidovic et al, ACM, 1997.

ART-UNIT: 212

PRIMARY-EXAMINER: Powell; Mark R.

ASSISTANT-EXAMINER: Das; Chameli C.

ATTY-AGENT-FIRM: Ratner & Prestia Townsend, Esq.; Tiffany L.

ABSTRACT:

A method for migrating legacy applications into a new software product architecture using a functional conversion module located within a system controller. The functional conversion module comprises a migration plan shut off. The functional conversion module further comprises three paths or branches through which a functional request can be routed. Functional requests which are not identified in the migration plan are routed through the first path and the functional request is sent to the pre-existing software and executed as requested. Functional requests identified in the migration plan for which the pre-existing software is in control are routed through the second path, and the functional request is sent to the pre-existing software and executed as received. In the background, the functional request is translated for the new software and sent to the new software and executed. Functional requests identified in the migration plan for which the new software is in control are routed through the third path, and the functional request is translated for the new software and sent to the new software and executed. If the pre-existing software has been shut off, the task is complete. If the pre-existing software is not identified as being shut off, the functional request is sent to the pre-existing software and executed as received in the background. Duplicate requests are suppressed by the system controller.

5 Claims, 4 Drawing figures

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Term	Documents
DATABASE	685007
DATABASIS	1
DATABASES	97434
(4 AND DATABASE).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	11
(L4 AND DATABASE).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	11

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1 Reticle enhancement technology trends: resource and manufacturability implications for the implementation of physical designs

Warren Grobman, Robert Boone, Cece Philbin, Bob Jarvis

April 2001 **Proceedings of the 2001 international symposium on Physical design**

Publisher: ACM Press

Full text available: pdf(510.15 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we briefly describe the lithography developments known as RET (Resolution Enhancement Technologies),which include off-axis illumination in litho tools,Optical and Process Correction (OPC), and phase shifting masks (PSM). All of these techniques are adopted to allow ever smaller features to be reliably manufactured, and are being generally adopted in all manufacturing below 0.25 microns. However, their adoption also places certain restrictions on layouts. We explore these res ...

2 Early verification of prototype tooling for IC designs

Pat Lamey

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation**

Publisher: IEEE Press

Full text available: pdf(282.28 KB) Additional Information: full citation, abstract, references, index terms

This paper presents an overview of IC manufacturing of design prototypes. The impact of manufacturing errors on the product development process is discussed. Alternative ways of reducing the impact of these errors are considered. Due to the increasing complexity of today's designs, manual inspection is no longer effective for early verification of prototype tooling. New, automatic inspection systems, which can verify tooling early in the manufacturing process are described. These ...

3 Addressing the requirements of a dynamic corporate textual information base

Peter G. Anick, Rex A. Flynn, David R. Hanssen

September 1991 **Proceedings of the 14th annual international ACM SIGIR conference on Research and development in information retrieval**

Publisher: ACM Press

Full text available: pdf(1.01 MB) Additional Information: full citation, references, citings, index terms

4 Semiconductor manufacturing: Automated material handling systems: a simulation-

based design framework for automated material handling systems in 300mm fabrication facilities
Dima Nazzal, Douglas A. Bodner
December 2003 **Proceedings of the 35th conference on Winter simulation: driving innovation**
Publisher: Winter Simulation Conference
Full text available: pdf(362.35 KB) Additional Information: full citation, abstract, references

This paper describes a methodology to tackle the problem of designing Automated Material Handling Systems (AMHS) for 300mm wafer fabrication facilities. The proposed framework divides the design process into two levels: architectural and elaborative. Prior to the design, fab data are preprocessed using simulation of manufacturing operations. The output data and fab requirements data are then profiled to aid in design decision making at the architectural level. Once architectural design decisi ...

5 Floorplanning: Multi-project reticle floorplanning and wafer dicing
Andrew B. Kahng, Ion M□ndoiu, Qinke Wang, Xu Xu, Alex Z. Zelikovsky
April 2004 **Proceedings of the 2004 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(313.16 KB) Additional Information: full citation, abstract, references, index terms

Multi-project Wafers (MPW) are an efficient way to share the rising costs of mask tooling between multiple prototype and low production volume designs. Packing the different die images on a multi-project reticle leads to new and highly challenging floorplanning formulations, characterized by unusual constraints and complex objective functions. In this paper we study multi-project reticle floorplanning and wafer dicing problems under the prevalent side-to-side wafer dicing technology. Our contrib ...

Keywords: multi-project wafers, reticle design, wafer dicing

6 Assessment of potential gains in productivity due to proactive reticle management using discrete event simulation
Sungmin Park, John Fowler, Matt Carlyle, Matt Hickie
December 1999 **Proceedings of the 31st conference on Winter simulation: Simulation--a bridge to the future - Volume 1**
Publisher: ACM Press
Full text available: pdf(121.69 KB) Additional Information: full citation, references, index terms

7 Semiconductor manufacturing: Automated material handling systems: automated reticle handling: a comparison of distributed and centralized reticle storage and transport
Anne M. Murray, David J. Miller
December 2003 **Proceedings of the 35th conference on Winter simulation: driving innovation**
Publisher: Winter Simulation Conference
Full text available: pdf(308.46 KB) Additional Information: full citation, abstract, references

The implementation of Automated Material Handling Systems (AMHS) in 300mm semiconductor facilities provides the opportunity to realize significant benefits in fabricator productivity and performance. The leverage associated with automated reticle delivery to photolithography process tools may be less apparent than a fab-wide AMHS. However, a high product mix environment requires the tracking, storage and transportation of thousands of reticles to successfully process wafers on photolithograph ...

8 Placement: Reticle floorplanning of flexible chips for multi-project wafers
Meng-Chiou Wu, Rung-Bin Lin
April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(333.42 KB) Additional Information: full citation, abstract, references, index terms

Multi-project wafer has become a low-cost avenue to gain access to more advanced process technology via amortizing mask cost among chips placed on the same reticle (called reticle floorplanning). Assuming chips have flexible dimensions, we propose a non-linear programming model for reticle floorplanning to optimize reticle area and make more chips with same width or height. The model allows co-existence of chips with fixed and flexible aspect ratios and can be solved within half an hour. For the ...

Keywords: dicing, mask cost, multi-project wafer, reticle floorplanning

9 AUTOSCHED AP by AutoSimulations
Tyler Phillips
December 1998 **Proceedings of the 30th conference on Winter simulation**
Publisher: IEEE Computer Society Press
Full text available: pdf(41.31 KB) Additional Information: full citation, references, index terms

10 Future Design Trends: A roadmap and vision for physical design
Andrew B. Kahng
April 2002 **Proceedings of the 2002 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(305.03 KB) Additional Information: full citation, abstract, references, citings, index terms

This invited paper offers "roadmap and vision" for physical design. The main messages are as follows. (1) The high-level roadmap for physical design is static and well-known. (2) Basic problems remain untouched by fundamental research. (3) Academia should not overemphasize back- filling and formulation over innovation and optimization. (4) The physical design field must become more mature and efficient in how it prioritizes research directions and uses its human resources. (5) The scope of physi ...

11 Semiconductor manufacturing: Simulation-based solution of load-balancing problems in the photolithography area of a semiconductor wafer fabrication facility
Lars Mönch, Matthias Prause, Volker Schmalfuss
December 2001 **Proceedings of the 33nd conference on Winter simulation**
Publisher: IEEE Computer Society
Full text available: pdf(230.41 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present the results of a simulation study for the solution of load-balancing problems in a semiconductor wafer fabrication facility. In the bottleneck area of photolithography the steppers form several different subgroups. These subgroups differ, for example, in the size of the masks that have to be used for processing lots on the steppers of a single group. During lot release it is necessary to distribute the lots over the different stepper groups in such a way that global targ ...

12 Design technology productivity in the DSM era (invited talk)
Andrew B. Kahng
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design**

automation

Publisher: ACM Press

Full text available: pdf(126.72 KB) Additional Information: full citation, abstract, references, index terms

Future requirements for design technology are always uncertain due to changes in process technology, system implementation platforms, and applications markets. To correctly identify the design technology need, and to deliver this technology at the right time, the design technology community - commercial vendors, captive CAD organizations, and academic researchers - must focus on improving design technology time-to-market and quality-of-result. Put another way, we must address the well-known ...

13 Reticle enhancement technology: implications and challenges for physical design

W. Grobman, M. Thompson, R. Wang, C. Yuan, R. Tian, E. Demircan

June 2001 **Proceedings of the 38th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(228.37 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we review phase shift lithography, rule vs. model based methods for OPC and model-based tiling, and discuss their implications for layout and verificat ion. We will discuss novel approaches, using polarizing films on reticles, which change the game for phase-shift coloring, and could lead to a new direction in c:PSM constraints on physical design. We emphasize the need to do tiling that is model-driven and uses optimization techniques to achieve planarity for better manufactu ...

Keywords: OPC, PSM, RET, mask data preparation, optical proximity correction, reticle enhancement technology, subwavelength lithography, tiling

14 Modeling the lot selection process in semiconductor photolithography processing

Thomas C. McGuigan

December 1992 **Proceedings of the 24th conference on Winter simulation**

Publisher: ACM Press

Full text available: pdf(351.05 KB) Additional Information: full citation, references, index terms

15 Session 1D:issues in timing estimation: Impact of systematic spatial intra-chip gate length variability on performance of high-speed digital circuits

Michael Orshansky, Linda Milor, Pinhong Chen, Kurt Keutzer, Chenming Hu

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(154.95 KB) Additional Information: full citation, abstract, references, citings

Using data collected from an actual state-of-the-art fabrication facility, we conducted a comprehensive characterization of an advanced 0.18μm CMOS process. The measured data revealed significant systematic, rather than random, spatial intra-chip variability of MOS gate length, leading to large circuit path delay variation. The critical path value of a combinational logic block varies by as much as 17%, and the global skew is increased by 8%. Thus, a significant timing error (~25%) ...

16 Semiconductor manufacturing: How "overstaffing" at bottleneck machines can unleash extra capacity

Robert C. Kotcher

December 2001 **Proceedings of the 33nd conference on Winter simulation**

Publisher: IEEE Computer Society
Full text available: pdf(315.46 KB) Additional Information: full citation, abstract, references, index terms

Using simulation, Headway Technologies predicted that increasing staffing among a group of already lightly loaded machine operators---"overstaffing"---would significantly improve throughput of its factory. This was counterintuitive since the operators already had significant idle time. Yet time studies confirmed that bottleneck equipment for which these operators were responsible was spending over 22% of its uptime idle solely due to lack of an operator. Analysis showed how this could be so: pro ...

17 Simulation in automated material handling systems design for semiconductor manufacturing
Gajanana Nadoli, Devadas Pillai
December 1994 **Proceedings of the 26th conference on Winter simulation**
Publisher: Society for Computer Simulation International
Full text available: pdf(713.86 KB) Additional Information: full citation, references, citings, index terms

18 CAD: Practical slicing and non-slicing block-packing without simulated annealing
Hayward H. Chan, Igor L. Markov
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(209.83 KB) Additional Information: full citation, abstract, references, index terms

We propose a new floorplanner BloBB based on multi-level branch-and-bound. It is competitive with annealers in terms of runtime and solution quality. We empirically quantify the gap between optimal slicing and non-slicing floorplans by comparing optimal packings and best seen results. Optimal slicing and non-slicing packings for *apte*, *xerox* and *hp* are reported. We also discover that the soft versions of all MCNC benchmarks, except for *apte*, and all GSRC benchmarks can ...

Keywords: block-packing, branch-and-bound, evaluation, floorplanning, hierarchical, large-scale, optimal, slicing, soft blocks

19 Operational simulation of an x-ray lithography cell: comparison of 200mm and 300mm wafers
K. Preston White, Walter J. Trybula
December 1999 **Proceedings of the 31st conference on Winter simulation: Simulation---a bridge to the future - Volume 1**
Publisher: ACM Press
Full text available: pdf(138.94 KB) Additional Information: full citation, references, index terms

20 The evolution of design automation to meet the challanges of VLSI
Lawrence M. Rosenberg
June 1980 **Proceedings of the 17th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(997.27 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the author's opinion of the major problems confronting Design Automation for VLSI and how Design Automation may evolve to meet these challenges. The paper first takes a historical look at the driving forces for Design Automation development by analyzing the evolution of Design Automation at RCA. It looks at both

some successful and unsuccessful development efforts and attempts to isolate some of the criteria necessary for success. It review RCA's current LSI Design Autom ...

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